Express Mail No.: EL 426 614 982 US

Patent Application for a New and Useful Invention Entitled:

ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT

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09571 "2268/60

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Attorney Docket No. 50944.9900

Client Docket No. 98RSS266

ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

The present invention is related to an electrostatic discharge (ESD) protection circuit, and more particularly to an ESD protection circuit designed for use in high frequency circuits.

2. BACKGROUND INFORMATION

Electrostatic charge is typically created by the contact and separation of two materials: many persons have felt the electrical shock that can occur when one touches a conducting surface after having walked across a carpet. These discharges commonly range between 2000 and 4500 volts and are discharged over a few milliseconds; they appear to the victim as an attention-getting, but harmless, electrical shock: the human body provides a high resistance to the discharge of these significant voltages, thereby decreasing the associated current. (The human body model standard assumes that the human body has a capacitance of 100 picofarads (pf) and a series resistance of 1500 ohms. Thus, the peak current flow during a human body ESD event is generally on the order of amps.)

The buildup of electrostatic charge may also occur when charges accumulate upon an ungrounded surface or an electrically non-conductive surface. For example, a piece of equipment, an electronic circuit, or the like, which is not grounded, may collect charges as it is moved from one location to

another. An electronic device sliding into or out of a bag can also generate an electrostatic charge. When the charged equipment touches an electrical conductor, an ESD event may occur. The electric current will follow the path of least resistance to the conductor. Unfortunately, the path of least resistance is often through vital electronic circuitry: In microelectronic systems, the conductor is often a prong of a packaged integrated circuit chip.

The wide-spread use of sensitive semiconductor chips in today's industrial and commercial products has made ESD protection a major concern in the design, layout, fabrication, and production of chips. Unlike the human body, which can easily dissipate an ESD event, semiconductor chips are extremely sensitive to ESD. Depending on the technology used in a chip, the maximum safe voltage the internal circuit elements can tolerate varies from approximately five volts to approximately twenty volts. As such, the mere touching of a chip by a non-grounded person or tool may result in an ESD event which can permanently damage the delicate electronic structures in an unprotected chip, possibly rendering the chip useless.

An ESD event through an integrated circuit (IC) can permanently damage the integrated circuit through several failing mechanisms, including the dielectric breakdown of oxides and other thin layers, the melting of conductive material such as polysilicon or aluminum, and the melting of semi-conductive material such as silicon, resulting in excessive leakage currents and open or short circuits in the IC.

To prevent ESD from damaging semiconductor circuits, various protective schemes may be employed. Large-scale protective schemes are often used to

protect system level equipment. Examples of these schemes include, but are not limited to, the following: electrical grounding of cases and external surfaces of the electrical equipment; electrical grounding of technicians via wrist bands; the prevention of electrostatic build-up through the use of static-safe clothing, static control shoes and high humidification; and the use of specialized shipping containers and storage bags. All of the above methods help to prevent the build-up of static charge. Additionally, small-scale, chip specific, approaches may be used. Often, high-current clamping devices are placed on the pins of a chip so that the high currents associated with an ESD event are safely shunted without away from the circuitry.

Ideally, such clamping devices are transparent during normal chip operations but shunt the high current of an ESD event away from the circuit being protected. This is typically accomplished by using an ESD protection device which is normally "off" but will turn on at a voltage that is well above a chip's normal operating voltage, but below a voltage that can damage the elements of an IC. When the ESD protection device is on, the excess current is passed through the ESD protection device instead of the current traveling through the circuit being protected.

While these circuits perform adequately in circuits that operate at low frequencies, they can adversely effect the operation of high frequency circuits.

The placement of an ESD protection circuit creates a large capacitance due to the ESD protection at the pad. The ESD parasitic capacitance becomes a significant problem around 1-2 GHz of operation; the reactance of the capacitance of a typical ESD protection circuit (1-2 pF) is almost as low as that of

the transmission line: it can be very difficult to make a resistive termination with such a large capacitive load. Therefore, a part of the signal is lost through the ESD protection circuit. As a result, high frequency devices often do not include any ESD protection.

Because ESD protection is just as important for high-frequency circuits as it is for lower-frequency circuits, there is a need for an on-chip ESD protection circuit that operates without adversely effecting the performance of the high-frequency circuit.

SUMMARY

The present invention is directed to a circuit placed between the source and a protected circuit. The circuit comprises a transmission line coupling the source and the protected circuit and a transistor connected in reverse mode between an electrical ground and the transmission line. The reverse mode transistor directs any abnormal currents through the reverse mode transistor, thus forcing electrostatic discharges charges away from the protected circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is further described in connection with the accompanying drawings, where like reference numbers depict like elements, in which:

Figure 1 depicts an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The circuit depicted in **Figure 1** is an embodiment of the present invention. This circuit is connected between an IC pad 118 at a lead 100 and the rest of a circuit connected at element 114. Transistor 202 is illustrated as an *npn*

transistor. The emitter 204 is connected between the IC pad and the circuit to be protected. The collector 206 is connected to a ground 210. The base 208 is connected to an optional resistor 212. The other end of resistor 212 is also connected to ground 210.

The circuit of Figure 1 operates in the following manner. When a large negative voltage is present at pad 100, the forward junction from base 208 to emitter 204 is turned on, creating, in effect, a short circuit between base 208 and emitter 204. Thus, the negative charge is delivered to ground 210 instead of traveling to the circuit being protected at 114.

When a large positive voltage is present at pad 100, there is a large voltage between emitter 204 and base 208, resulting in a "soft" breakdown of the *pn* junction. Preferably, this breakdown occurs at a voltage higher than the operating voltage of the circuit to be protected. The transistor is then operating in the inverse or reverse mode. Collector 206 acts as an emitter and emitter 204 acts as a collector. However, the gain, β, of this transistor in the reverse mode is low, about 4 or 5, as opposed to a β of about 100 for a transistor connected in the typical configuration. The junction between the emitter and the base becomes forward biased; *i.e.*, the transistor is in reverse operation mode. The current is shunted through collector 206 when the base voltage is greater than the collector voltage by about 0.7 volts. Thus, the current caused by the high voltage present at the input is shunted through emitter 204 to collector 206 to ground. Resistor 212 acts to cause a voltage drop between ground 210 and base 208. Resistor 212 may not be necessary if the intrinsic resistance of

transistor 202 is sufficiently large to maintain an appropriate base voltage greater than the voltage at collector 206.

Transistor 202 is preferably configured such that the breakdown voltage BV_{ebo} is higher than the operating voltage of the circuit being protected. However, BV_{ebo} must be lower than the breakdown voltage of the circuit being protected. In addition, the leakage current of ESD below BV_{ebo} must be very low.

In **Figure 1**, the capacitance, C_{be}, between the base 208 and the emitter 204, C_{be} is indicated by capacitor 216. Because of the configuration of transistor 202, the value of C_{be} is approximately 10 times less than the value of C_{js}. Thus, the high frequency performance is much improved. Thus, the response at high frequencies is greatly improved as compared to the circuit of Figure 1.

The present invention thus provides for a method for protecting a circuit from electrostatic discharges through the connection of a transistor in the reverse mode between a protected circuit and a pad coupled to the protected circuit, where the pad couples the protected circuit to, for example,

The above description presents the best mode contemplated in carrying out the invention. The techniques described above are, however, susceptible to modifications and alternate constructions from the embodiments shown above. For example, while the invention has been described with respect to an *npn* bipolar junction transistor (BJT), it should be appreciated that this invention can also operate with a *pnp* BJT. Furthermore, while this invention has been described with respect to high-frequency operation, it should be appreciated that the present invention will operate at any frequency and is thus appropriate for low-frequency circuits as well.

Consequently, it is not the intention to limit the invention to the particular embodiments disclosed. On the contrary, the invention is intended to cover all modifications and alternate constructions falling within the scope of the invention, as expressed in the following claims when read in light of the description and drawings.